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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,561	10/08/2003	Roger Lin	VIAP0075USA	2560

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EXAMINER	
NGUYEN, JOHN B	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,561	LIN, ROGER	
	Examiner	Art Unit	
	John B Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-13,15-23 and 25-30* is/are rejected.

7)☒ Claim(s) *4,14 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

OATH or DECLARATION

1. The new COMBINED DECLARATION AND POWER OF ATTORNEY is requested for replacement because the original COMBINED DECLARATION AND POWER OF ATTORNEY is un-readable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-3, 5-10, 11-13, 15-20, 21-23, and 25-30 are rejected under 35 U.S.C. 102(a) as being anticipated by APPLICANT'S PRIOR ART.

3. Regarding to claim 1, APPLICANT'S PRIOR ART (Fig. 1 and Fig. 2) disclose a converter (10, digital-to-analog) for providing an output voltage (Vp) according to an input code (26), the converter comprising: a control logic (12) for generating a positive control code (Yp0-Yp2) and a negative control code (Xp0-Xp2) according to the input code (26); a positive electrical module (16A) for providing a positive current (18A-18C) corresponding to the positive control code (Yp0-Yp2) to an output (Na); a negative electrical module (16B) for providing a negative current (20A-20C) corresponding to the negative control code (Xp0-Xp2) to the output (Na); and an assistant electrical module (20D and 22 combined) for providing a non-zero current

to the output (Na) when the negative electrical module provides the negative current to the output (Na, when switch Co is closed).

4. Regarding to claim 2, the converter of claim 1, wherein the input code (26) includes a sign code (Ap3) and a value code (Ap0-Ap2).

5. Regarding to claim 3, the converter of claim 2, wherein when the sign code (Ap3) corresponds to a predetermined negative sign code (Fig. 2, Ap3), the control logic (12) encodes the value code (Ap0-Ap2) as the negative control code (Xp0-Xp2) by a first coding method (Fig. 2); and when the sign code (fig. 2, Ap3) does not correspond to the predetermined negative sign code (fig. 2), the negative control code (Xp0-Xp2) generated by the control logic (12) prevents the negative electrical module (16B) from providing the negative current (Fig. 2, 28B).

6. Regarding to claim 5, the converter of claim 2, wherein when the input code (26) represents a first negative input code (fig. 2, 26), the first negative input code is encoded by a second coding method (Fig. 2, 28B), the second coding method being twos complement arithmetic coding (Paragraph 0007, lines 7-17).

7. Regarding to claim 6, the converter of claim 1, wherein the assistant electrical module (20D) comprises a unit current source (Fig. 1) and each current (20A-20C) provided by the negative electrical module (16B) is a multiple of the unit current (1I-4I).

8. Regarding to claim 7, the converter of claim 1, wherein if the input code (26) is a first positive input code (Fig. 2, 26), the control logic (12) generates a first positive control code (28A) and a first negative control code (28B) according to the first positive input code, the first negative control code preventing the negative electrical module (16B) from providing the

negative current to the output (Na, switch 22 is opened).

9. Regarding to claim 8, the converter of claim 1, wherein if the input code (26) is a first negative input code (Fig.2, 26), the control logic (12) generates a second positive control code (28A) and a second negative control code (28B) according to the first negative input code, the second positive control code preventing the positive electrical module from providing the positive current to the output (Na, switch 22 is closed).

10. Regarding to claim 9, the converter of claim 1, wherein the positive control code (28A) comprises a plurality of positive control bits (Yp0-Yp2), the positive electrical module (16A) having a plurality of positive current sources (18A-18C), each positive current source corresponding to a positive control bit (Yp0-Yp2) in order to provide a positive current to a first node (Na) according to the positive control bit, and the negative control code (28B) comprises a plurality of negative control bits (Xp0-Xp2), the negative electrical module (16B) having a plurality of negative current sources (20A-20C), each negative current source corresponding to a negative control bit (Xp0-Xp2) in order to provide a negative current to the first node (Na) according to the negative control bit.

11. Regarding to claim 10, the converter of claim 9, wherein the negative current sources (20A-20C) of the negative electrical module (16B) separately correspond to the positive current sources (18A-18C) of the positive electrical module (16A), the negative current sources providing negative current (Para. 0006, lines 22-23) and the positive current sources providing positive current (Para. 0006, lines 26-27), the magnitude of the negative current being the same as that of the positive current (Para. 0010, lines 1-3), the phase of the negative current being opposite that of the positive current (Para.0010, line 4).

12. Regarding to claim 21, an electrical module (10, digital-to-analog) used in a converter for providing an output voltage (Vp) according to an input code (26), the input code including a sign code Ap3) and a value code (Ap0-Ap2), the electrical module comprising: a positive electrical module (16A) for providing a positive current (18A-18C) to an output (Na) according to a positive control code (Yp0-Yp2); a negative electrical module (16B) for providing a negative current (20A-20C) to the output (Na) according to a negative control code (Xp0-Xp2); and an assistant electrical module (20D) for providing a constant current to the output (Na) when the negative electrical module provides a negative current to the output (Na, when switch 22 is closed).

13. Regarding to claim 22, the electrical module of claim 21 further comprising a control logic (12) for generating the positive control code (Yp0-Yp2) and the negative control code (Xp0-Xp2) according to the input code (26).

14. Regarding to claim 23, the electrical module of claim 22, wherein when the sign code (Ap3) corresponds to a predetermined negative sign code (Fig. 2, Ap3), the control logic (12) encodes the value code (Ap0-Ap2) as the negative control code (Xp0-Xp2) by a first coding method (Fig. 2); and when the sign code (Fig. 2, Ap3) does not correspond to the predetermined negative sign code (Fig. 2, Ap3), the negative control code (Xp0-Xp2) generated by the control logic (12) prevents the negative electrical module (16B) from providing the negative current (Fig. 2, 28B).

15. Regarding to claim 25, the electrical module of claim 22, wherein when the input code (26) represents a first negative input code (Fig. 2, 26), the first negative code is encoded by a second coding method (Fig. 2, 28B), the second coding method being twos complement

arithmetic coding (Para. 0007, lines 7-17).

16. Regarding to claim 26, the electrical module of claim 21 wherein the assistant electrical module (20D) corresponds to a unit current source (Fig. 1) and current provided by the negative electrical module (16B) is a multiple of the unit current (1I-4I).

17. Regarding to claim 27, the electrical module of claim 21, wherein if the input code (26) is a first positive input code (Fig. 2, 26), a first negative control code (28B) is generated according to the first positive input code (Fig. 2, 26), the first negative control code preventing the negative electrical module (16B) from providing a negative current to the output (Na, when switch 22 is opened).

18. Regarding to claim 28, the electrical module of claim 21 wherein if the input code is a first negative input code (Fig. 2, 26), a positive control code (28A) is generated according to the first negative input code (Fig. 2, 26), the positive control code preventing the positive electrical module (16A) from providing a positive current to the output (Na, when switch 22 is closed).

19. Regarding to claim 29, the electrical module of claim 21 wherein the positive control code (28A) comprises a plurality of positive control bits (Yp0-Y2p), the positive electrical module (16A) having a plurality of positive current sources (18A-18C), each positive current source corresponding to a positive control bit in order to provide a positive current to a first node (Na) according to the positive control bit (Yp0-Yp2), and the negative control code (28B) comprises a plurality of negative control bits (Xp0-Xp2), the negative electrical module (16B) having a plurality of negative current sources (20A-20C), each negative current source corresponding to a negative control bit in order to provide a negative current to the first node

(Na) according to the negative control bit (Xp0-Xp2).

20. Regarding to claim 30, the electrical module of claim 29 wherein the negative current sources (20A-20C) of the negative electrical module (16B) separately correspond to the positive current sources (18A-18C) of the positive electrical module (16A), the negative current sources providing negative current (Para. 0006, lines 22-23) and the positive current sources providing positive current (Para. 0006, lines 26-27), the magnitude of the negative current being the same as that of the positive current (Para. 0010, lines 1-3), the phase of the negative current being opposite that of the positive current (Para. 0010, line 4).

21. Regarding to method claims 11-13 and 15-20, the apparatus claims 1-3 and 5-10 discussed above would perform the claims of method 11-13 and 15-20.

ALLOWABLE SUBJECT MATTERS

22. Claims 4, 14 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (See enclosed Form PTO-892).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B Nguyen whose telephone number (571) 272-1808. The examiner can normally be reached on 8AM-4: 30 PM M-F.

John B. Nguyen
March 04, 2004